Radio Shack®

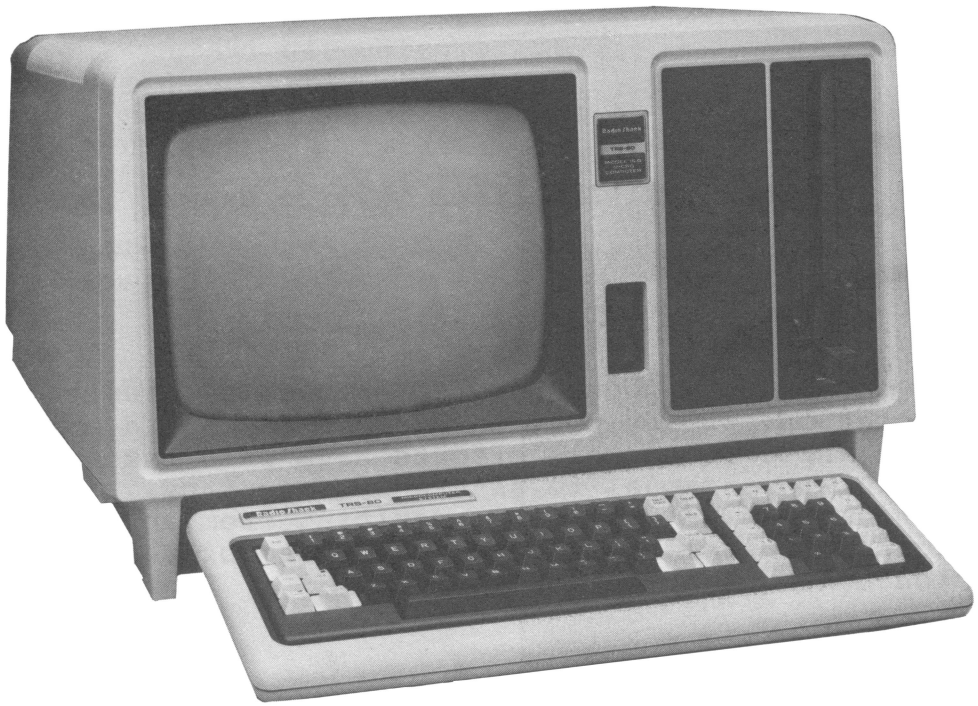
Service Manual

26-6013

TRS-80®

Multiterminal Interface

Catalog Number 26-6013



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TRS-80® Multiterminal Interface Service Manual

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1/ General

The Multiterminal Interface Board (26-6013) allows the Model 16/16B to interface with up to three additional terminals. This capability, combined with the XENIX OS multitasking capability, allows up to six independent operators to have access to the features contained in a single Model 16/16B. This results in a cost savings per terminal and the added advantage of a shared data base.

The Multiterminal Interface Board is basically a three-port RS-232C serial interface to the 8-bit Z80A Model 16/16B Peripheral Processor.

The normal mode of operation as defined by software is full duplex, asynchronous transmission with a baud rate range from 50 to 9600. The computer interface is interrupt driven. On the reception or transmission of any character, an interrupt is created and the character is stored to or retrieved from a memory buffer.

The Multiterminal Interface Board is mounted in the Card Cage assembly which is internal to the Computer. Since the Multiterminal Interface Board must be in the interrupt chain, its priority position in the card cage must be as noted in the chart below to preserve this daisy-chaining action. If one of the boards listed in the first three positions is not present, then the other boards move up a slot. If a board position is not critical, i.e. it is not a part of the interrupt cycle, its priority position is noted as "None". Physical positioning of the board in the card cage in the Model 16B is from the bottom (J1) to the top (J7).

Priority Pos.	Description	Priority
1	ARCNET	1
2	Hard Disk Interface	2
3	Multiterminal Interface	3
4	Graphics	None
5	Video/Keyboard Interface	None
6	256K Memory Board	None
7	256K Memory Board	None
8	256K Memory Board	None
9	16 Bit CPU Board	None

2/ Installation

Included in the following pages are instructions for installing and interconnecting the Multiterminal Interface PCB in the Model 16 Radio Shack Computer. This option allows you to interconnect as many as five additional terminals to the computer so that a common data base may be used by all terminals. Refer to the TRS-XENIX Operator's Manual for operating instructions for the system.

2.1. Software Requirements

The only current operating system offered by Radio Shack which supports this board is TRS-XENIX, Version 01.03.00 or higher. You must upgrade your system to at least a version 01.03.00.

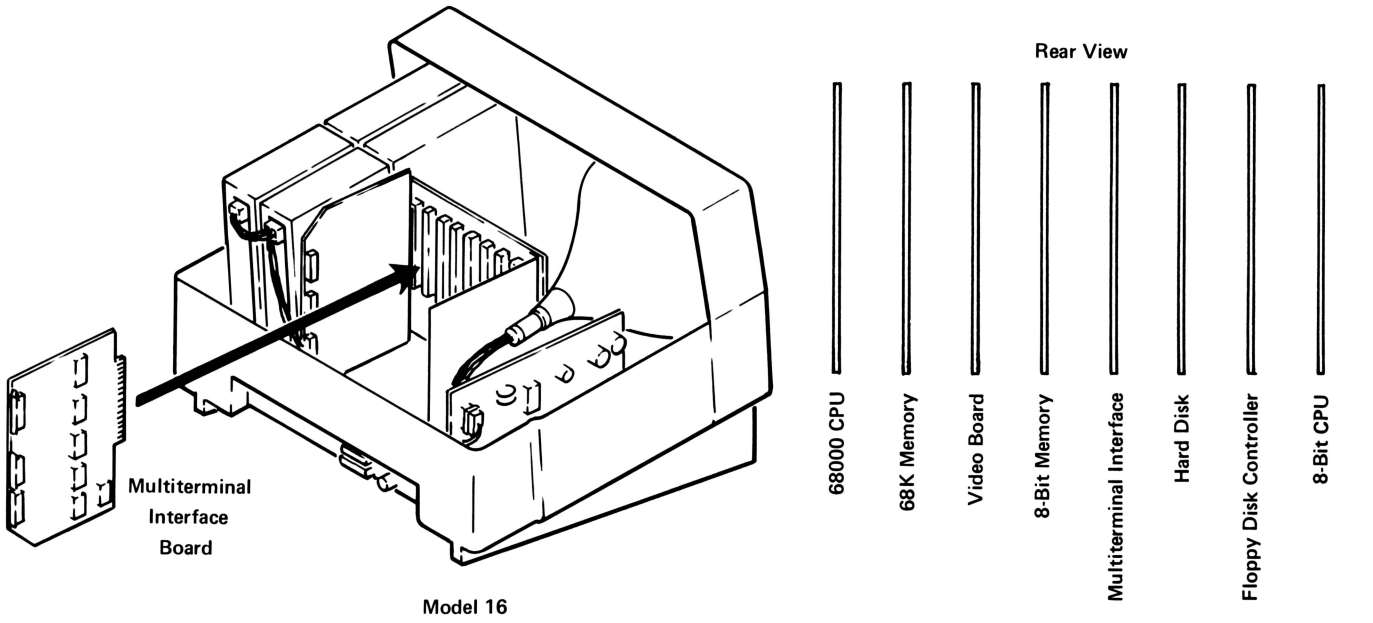
If you already have the XENIX Operating System, it is necessary to modify it using a software update diskette (Catalog No. 700-2066) which modifies a 1.1 or 1.2 system to a version 01.03.00 System.

If you do not have the XENIX Operating System, it will be necessary to purchase the XENIX Version 01.03.00 Core System (Catalog No. 700-2052).

2.2. Installation

The following instructions are given to allow proper installation of the Multiterminal Interface Board, check out its function to ensure proper operation, and perform modifications required to the Main Terminal to allow communication between it and the remote terminal(s).

The Multiterminal Interface Board is installed in a Model 16 or 16B in the card cage assembly. It is accessible when the rear cover is removed from the Model 16B Case Assembly, or the top cover from the Model 16.



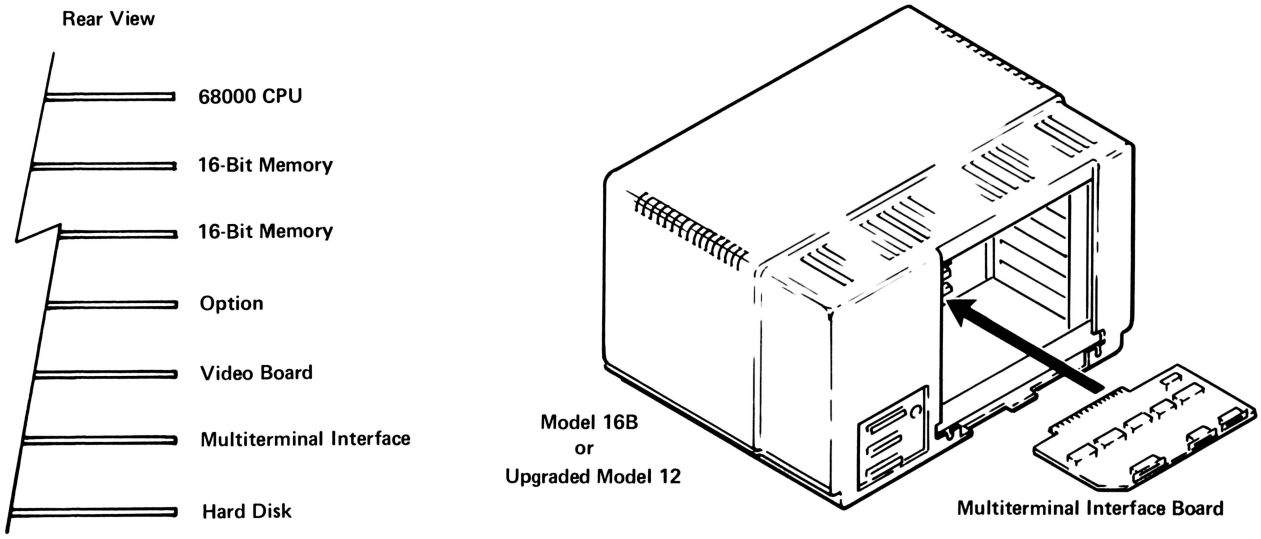


Figure 2-1. Multiterminal Interface Board Installation

1. Rear Cover Removal

Model 16

Turn the computer so that the rear is facing you to allow access to the top cover. Remove the top cover by unscrewing the two mounting screws. Lift up and to the rear on the top cover to gain access.

Insert Multiterminal Interface PCB as noted in Figure 2-1.

Model 16B

Turn the computer so that the rear is facing you to allow access to the rear cover. Remove the two mounting screws at the lower part of the rear cover. Lift out on the bottom of the cover plate and pull down.

2. Remove the card holding brackets from either side of the card cage to allow the Multiterminal Interface board to be installed. Attach the cable end(s) to the connector(s) on the Multiterminal Interface Board. The DIP switch S1 must be set for the proper operation as noted in Figure 2-2. Slide the board into the connector slot as shown in Figure 2-1. The Multiterminal Interface board must be in the interrupt chain. Therefore, there must be no empty slots between the board and J1. The Multiterminal Interface board must be in J1 if no other boards are present.

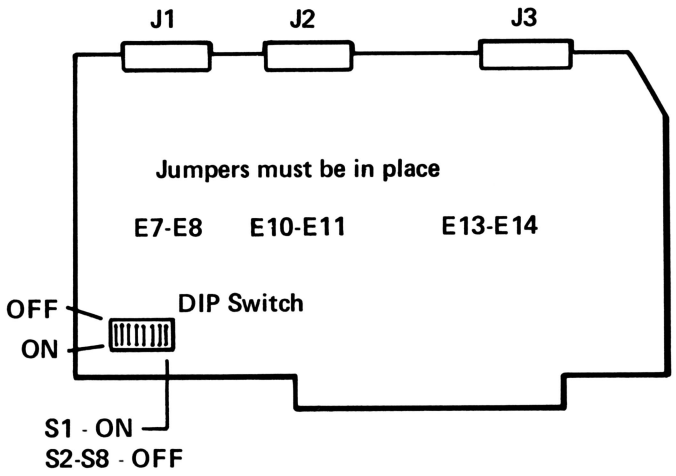


Figure 2-2. DIP Switch Settings

3. Loosen the screws which mount the Strain Relief Bracket to the Rear Door. Feed the cable(s) from the remote unit(s) between the Strain Relief Bracket and the Rear Door and tighten the screws mounting the Bracket. Allow enough cable to the inside of the bracket to provide an internal loop.

2.3. Setting Up Multiple Terminals

The Xenix system is programmed to accommodate a wide range of terminal types -- but the system has to know what kind of terminals are connected to it so that it can calibrate itself to the terminal's particular characteristics and capabilities.

The console is automatically set to accommodate two DT-1 terminals. TRS-XENIX calls them the "Adds25" terminal type, and expects the terminals you connect to be set to the DT-1's Adds25 emulation mode. That information is stored in a TRS-XENIX file called /etc/ttytype. If you're connecting a DT-1 to the console, just follow connection instructions and proceed directly to enabling your terminal (see Paragraph 2.6). If, however, you're connecting a terminal other than a DT-1, you have to let TRS-XENIX know.

A file called /etc/termcap stores the characteristics of all commonly used terminals. The following list gives the names and codes for the terminals pre-configured in /etc/termcap:

NAME	CODE
VT 100	vt100
VT 52	vt52
ADM 3a	adm3a
ADM 5	adm5
Televideo 910	tvi910
ADDS 25	adds25

To let TRS-XENIX know what kind of terminal you'll be using, edit the /etc/ttytype file to include one of the above names. At that point, TRS-XENIX can work with your terminal -- just as soon as you've enabled it.

2.4. Connecting A Terminal To The Computer (see Figure 2-3)

First, check which connector you're using for the terminal. If it is either Serial Channel A or B, you will need an RS-232 cable (Cat. No. 26-4403) and a null modem adapter (Cat. No. 26-1496) for each terminal.

1. Connect one end of the RS-232 cable to the terminal's RS-232 jack.

2. Connect the other end of the cable to the female plug of the null modem adapter.

3. Connect the adapter's male plug to either Serial Channel A or B of your computer.

4. If the computer requires it (check the owner's manual), insert a Terminator Plug into any unused Serial Channel.

If the terminal connects to one of the three connectors on the Multiterminal Interface PCB, you will need only the RS-232 cable assembly.

2.5. Checking Installation

Correct installation of the Multiterminal Interface is ensured when the following commands typed into the computer running XENIX produce the noted responses.

Type in the following command*:

```
disable tty0X (enter)
```

Response

There will be no response or the following error message will appear:

```
disable: tty0X is already disabled
disable: /etc/ttys not updated     (which is OK)
```

* 0X = one of the tty terminals, either 4, 5 or 6. For example, tty04.

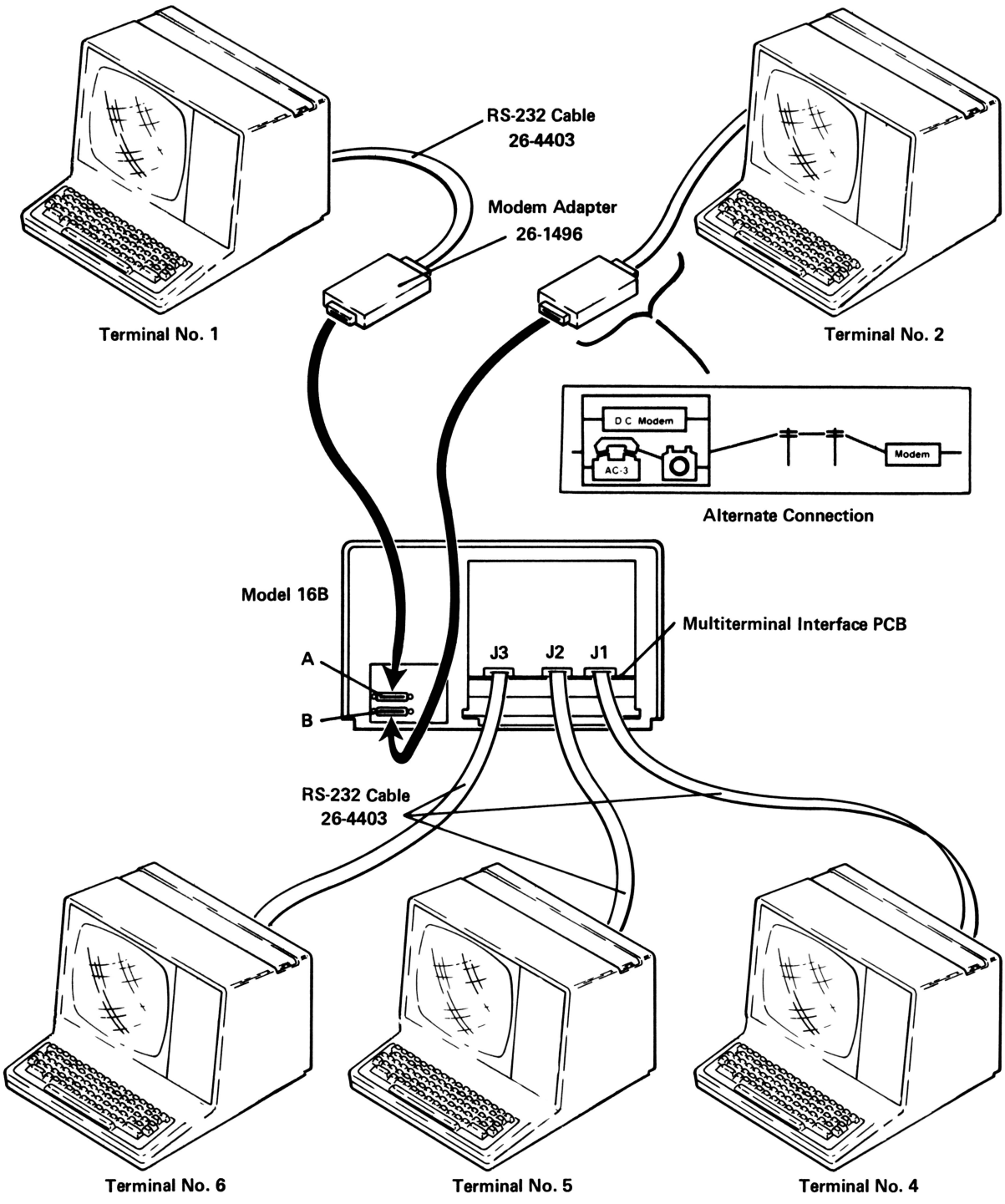


Figure 2-3. Typical Installation, Multiterminal Interface Board

Type in the following command:

```
cat /etc/ttys >/dev/tty0X (enter)
```

Response (on terminal 0X)

```
lhconsole
09tty01
09tty02
09tty04
09tty05
09tty06
```

(or something similar -- it should look the same as if "cat /etc/ttys" were typed without any output redirection)

2.6. Enabling A Terminal

Before you can use a terminal, it must be enabled. To enable a terminal connected at Serial Channel A, type:

```
enable tty01 <ENTER>
```

To enable a terminal connected at Serial Channel B, type:

```
enable tty02 <ENTER>
```

For any terminals connected to the Multiterminal Interface PCB, type:

```
enable tty04 <ENTER>     (for terminal connected
                          to J1)
  or
enable tty05 <ENTER>     (for terminal connected
                          to J2)
  or
enable tty06 <ENTER>     (for terminal connected
                          to J3)
```

Then you're ready to use the terminal with TRS-XENIX.

2.7. Disabling A Terminal

If you have to disconnect a terminal from the main computer for any reason, be sure you first disable it. Again, check the connector the terminal is using, and at the main terminal type:

```
disable tty01          (for Serial Channel A)

  thru

disable tty06          (for terminal connected
                        to J3)
```

(Remember: There is no tty03)

and proceed to disconnect the remote terminal connector from the main computer connector.

2.8. Model II to 16 Conversions

The Model II can be used to test the Multiterminal Interface board provided some precautions are taken.

There is a dual addressing problem in early Model II VDG boards that makes ports 7CH-7FH be interpreted as ports FCH-FFH. This is only on Rev A and Rev B VDG boards. To correct this, a jumper has to be installed from pin 1 to pin 10 of IC27 on the VDG board. This will not affect the normal operation of the Model II.

The test software MULTERM for the Multiterminal Interface board was written for ports 70H-7EH. TRS-XENIX also uses 70H-7EH for the first board. If this is in an older Model II with a Rev A or Rev B VDG board OR if a Model II/12/16/16B has an older video board installed, it will cause a problem testing the board or attempting to run TRS-XENIX without the jumper mentioned above on these older VDG boards.

3/ Theory Of Operation

The Multiterminal Interface Board can be functionally divided into five parts: (1) USART circuitry; (2) Baud Rate Generator; (3) RS-232C Interface circuitry; (4) Loopback; and (5) Z80 Interface. See Intel Specification 8251A and Model II Technical Reference Manual, SIO Section.

3.1 USART Circuitry

The USART (Universal Synchronous Asynchronous Receiver Transmitter) is a Medium Scale Integrated Circuit (MSI) which accomplishes all of the required transformation of serial and parallel data under CPU directions. The USART circuit can be divided into four parts: (1) the CPU interface logic; (2) the Transmitter logic; (3) the Receiver logic; and (4) the Modem Control logic. The schematic designators for the USARTs are U16, U17, and U19.

3.1.1 CPU Interface Logic

The CPU Interface logic links the two major parts -- the transmitter and the receiver -- with the Z80 CPU. The Z80 CPU, by read/write operations, issues configuration/ parameter commands and transmitter data, and reads status and receiver data. Configuration commands, for example, specify the transmission mode (asynchronous) and transmission characteristics (number of characters, stop bits, etc.). See Table 3-1 for the programming parameters.

3.1.2 Transmitter Logic

The transmitter serially shifts out the character data stored in the transmitter buffer at the applied baud clock rate. When the transmitter buffer is empty, it sets the TX RDY signal. The TX RDY signal is connected to an interrupt which is used to request another character from the CPU. Transmission is controlled either internally by the TX Enable flag controlled by the CPU or possibly by external RS-232 signals DSR/DCD and CTS received by the modem control logic.

BAUD RATE GENERATOR	
ADDRESS	DATA
70	CHANNEL 0, LSB BYTE, MSB BYTE
71	CHANNEL 1, LSB BYTE, MSB BYTE
72	CHANNEL 2, LSB BYTE, MSB BYTE
73	COMMAND WORD

COMMAND WORD

7	6	5	4	3	2	1	0
				0	1	1	0
00: SELECT CHANNEL 0 01: SELECT CHANNEL 1 10: SELECT CHANNEL 2		00: LATCH CURRENT COUNT VALUE TO READ 11: LOAD COUNTER VALUE		COUNTER OUTPUT SIGNAL CONTINUOUS PULSE 50% DUTY CYCLE			COUNTER DATA TYPE 0=BINARY 1=BCD

Note 1: Bit 4, 5 = 0, Bit 0-3 = DON'T CARE

Note 2: Counter Value Read/Write in two consecutive bytes, LSB first.

Table 3-1. Programming Parameters (page 1 of 4)

INTERRUPT CONTROLLER	
ADDRESS	DATA
74	CHANNEL 0 CTC CONTROL/INTERRUPT VECTOR
75	CHANNEL 1 CTC CONTROL/INTERRUPT VECTOR
76	CHANNEL 2 CTC CONTROL/INTERRUPT VECTOR
77	NOT USED

CONTROL WORD:

7	6	5	4	3	2	1	0
							1
INTERRUPT ENABLE 0 = DISABLE	MODE 0 = TIMER 1 = COUNTER	PRESCALER VALUE 0 = 16 1 = 256	CLOCK/TRIGGER EDGE 0 = FALL 1= RISE	TIMER TRIGGER 0 = AUTO 1 = CLOCK/ TRG	1 = TIME CONSTANT BYTE FOLLOWS (TIMER MODE)	0 = CONTINUOUS OPERATION 1 = RESET	1= CONTROL WORD 0= INTERRUPT VECTOR

TIME CONSTANT:

MSB		LSB

INTERRUPT VECTOR:

		0
VECTOR DATA	CHANNEL ID 00 = CHANNEL 0 01 = CHANNEL 1 10 = CHANNEL 2 11 = CHANNEL 3	INSERTED BY CTC

Table 3-1. Programming Parameters (page 2 of 4)

USART	
ADDRESS	DATA
78	CHANNEL 0, RECEIVE, TRANSMIT CHARACTER
7A	CHANNEL 1, RECEIVE, TRANSMIT CHARACTER
7C	CHANNEL 2, RECEIVE, TRANSMIT CHARACTER
79	CHANNEL 0, USART MODE/COMMAND/STATUS
7B	CHANNEL 1, USART MODE /COMMAND/STATUS
7D	CHANNEL 2, USART MODE/COMMAND/STATUS

MODE

7	6	5	4	3	2	1	0
		0	0			1	0
STOP BIT NUMBER 00 = INVALID 01 = 1 10 = 2 11 = 3		0 = ODD PARITY 1 = EVEN PARITY	PARITY ENABLE = 1	CHARACTER LENGTH 00 = 5 01 = 6 10 = 7 11 = 8		SYNC/ASYNC & BAUD RATE FACTOR 00 = SYNC 01 = 6 10 = 16X 11 = 64X	

COMMAND

0							
	1 = RESET IC	1 = RTS TRUE	1 = RESET ERROR	0 = NORMAL 1 = BREAK	1 = ENABLE RECEIVE	1 = DTR TRUE	1 = ENABLE TRANSMIT

Table 3-1. Programming Parameters (page 3 of 4)

USART (con't)	
ADDRESS	DATA

79, 7B, 7D (con't) STATUS

7	6	5	4	3	2	1	0
1 = DSR TRUE	1 = RX DATA = BREAK	1 = FRAME ERROR	1 = OVERRUN	1 = PARITY ERROR	1 = TX EMPTY	1 = RX RDY TRUE	1 = TY RDY TRUE

7E	LOOPBACK COMMAND

LOOPBACK COMMAND

X	X	X	X	X	X	X	
							1 = LOOPBACK

7F	NOT USED

Table 3-1. Programming Parameters (page 4 of 4)

3.1.3 Receiver Logic

The receiver serially shifts serial data in, using the applied baud clock (in this particular operation, it is multiplied sixteen times). When the "start" bit sequence is detected, the next data character bits are stored in the receive buffer. When a complete character is stored, the RX RDY signal is set. The RX RDY signal is applied to an interrupt (the same interrupt as the TX RDY) requesting the CPU to read the character. Reception is controlled by the RX Enable flag and reception of data character.

3.1.4 Modem Control Logic

The Modem Control logic handles the RS-232C handshaking signals DSR/DCD, DTR, CTS, and RTS. The state of the source signals DTR and RTS is controlled by the Z80 CPU. These four signals are used to control the flow of data around the dedicated link.

3.2 Baud Rate Generator

The Baud Rate Generator U18 is an MSI IC that consists of three independent programmable counters. Each counter is hard-wired to a specific USART. The counter output is applied to the USART TX and RX clocks. The frequency output of each counter is a fractional portion of the applied clock frequency. The fraction is programmed individually into each counter by the CPU (therefore, each can have a different baud rate frequency). The input clock is 2.000 MHz divided from the 4 MHz on the Z80 bus. The BCD values for the different baud rate frequencies are noted in Table 3-2. See Intel Specification 8253.

3.3 RS-232C Interface

The RS-232C Interface logic consists of buffers and receivers which convert from/to the digital logic levels to the +/-12 Vdc levels of the RS-232C. The buffers are the 1488 ICs U2, U4, and U7. The buffers which transmit the data and clocks have a capacitor on their output. The purpose of this capacitor is to increase the rise time of the signals to reduce cross-coupling. The receivers are the 1489 ICs U1, U3, and U6. The receivers for the control signals have resistor terminations to one of the power

8253 BAUD RATE GENERATOR

(CLOCK = 2.000 MHz)

BAUD RATE	1X		16X		64X	
	DEC	HEX	DEC	HEX	DEC	HEX
50	40,000	9C40	2,500	09C4	625	0271
75	26,667	682B	1,667	0683	417	01A1
110	18,182	4706	1,136	0470	284	011C
150	13,333	3415	833	0341	208	00D0
300	6,667	1A06	417	01A1	104	0068
600	3,333	0D05	208	00D0	52	0034
1200	1,667	0683	104	0068	26	001A
2400	833	0341	52	0034	13	000D
4800	417	01A1	26	001A	7	0007
9600	208	00D0	13	000D	3	0003

Table 3-2. Baud Rate Generator

supply voltages. This biases the signal into either the "true" (-12 Volts) or "false" (+12 Volts) state to create the required state if the signal is not present.

3.4 Loopback Circuit

The loopback circuitry provides a means to self-test the three serial channels without external stimulus. The output serial data TXD and the modem control signals DTR and RTS of the USARTs are returned to their complementary signals RXD, DSR/DCD, and CTS. This is done before the RS-232 interface to switch the signals at digital levels. All three loopback switches U9, U10, and U13 are switched on/off together.

3.5 Processor Interface

The processor interface consists of an address decoder, control signal circuitry, data transceiver, interrupt controller and clock circuitry.

3.5.1 Address Decoder

The address decoder determines whether or not the Z80 is addressing the Multiterminal Interface. U24 is a line receiver. U21 decodes A7-A4 into one-of-eight addresses. Switch SW1, manually set, selects one of the outputs to be "ADDMATCH" which, when combined with IOR/IOW in U22 (a programmable logic array), creates the individual chip selects CS*.

3.5.2 Control Signal Circuitry

The control signal circuitry consists of line receiver U25, timing signal converter U8, U12, and U15 and loopback control U5. The timing signal converter delays the leading edge of the Z80 signals IORQ, IOR, and IOW with respect to the chip selects to be acceptable by the INTEL family ICs.

3.5.3 Data Transceiver

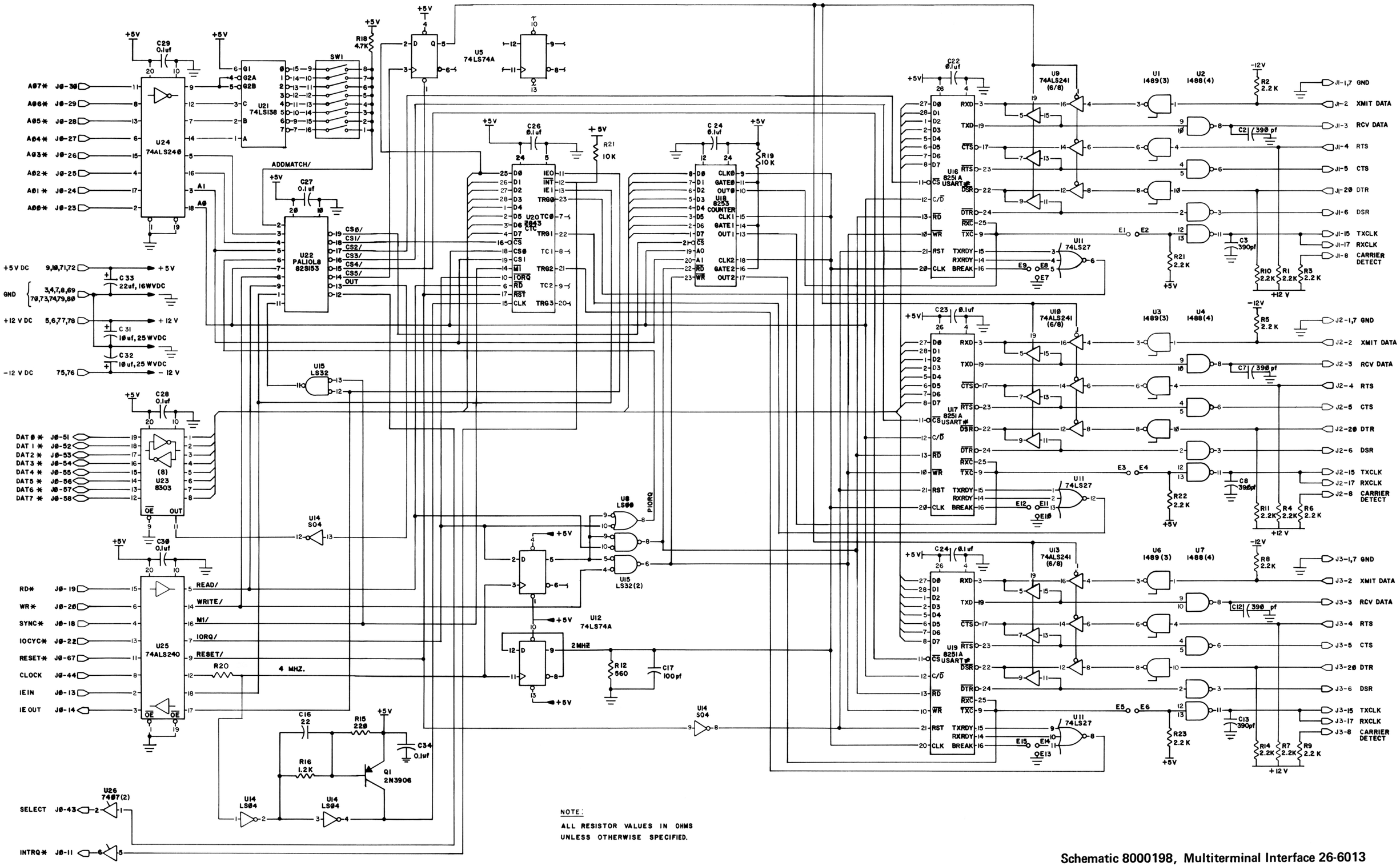
The data transceiver is U23. Direction is controlled by an output from U22, labeled "OUT". The normal direction is receive (or IN). When OUT=1, the direction is onto the Z80 bus.

3.5.4 Interrupt Controller

The interrupt controller U20 is a Z80 CTC to match the existing interrupt format. The TX RDY, RX RDY and BREAK (selectable) of each USART are ORed together to create a single interrupt per USART channel. This interrupt is used to inform the CPU when a USART needs service.

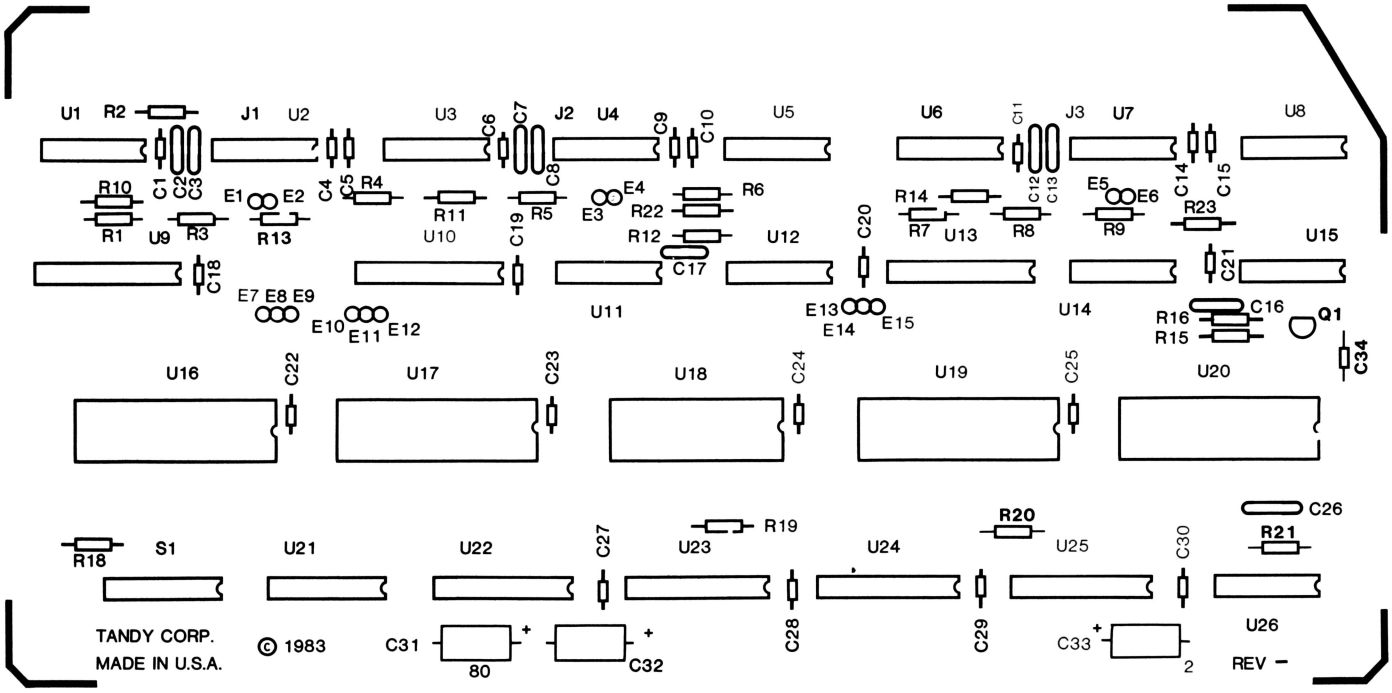
3.5.5 Clock Circuitry

The clock circuitry has two parts. First, the 4 MHz clock from the bus is divided by 2 to create a 2 MHz clock. This clock is used in two places: the unbuffered version is applied to the baud rate generator U18; the buffered version is increased in amplitude to meet Z80 CTC requirements.

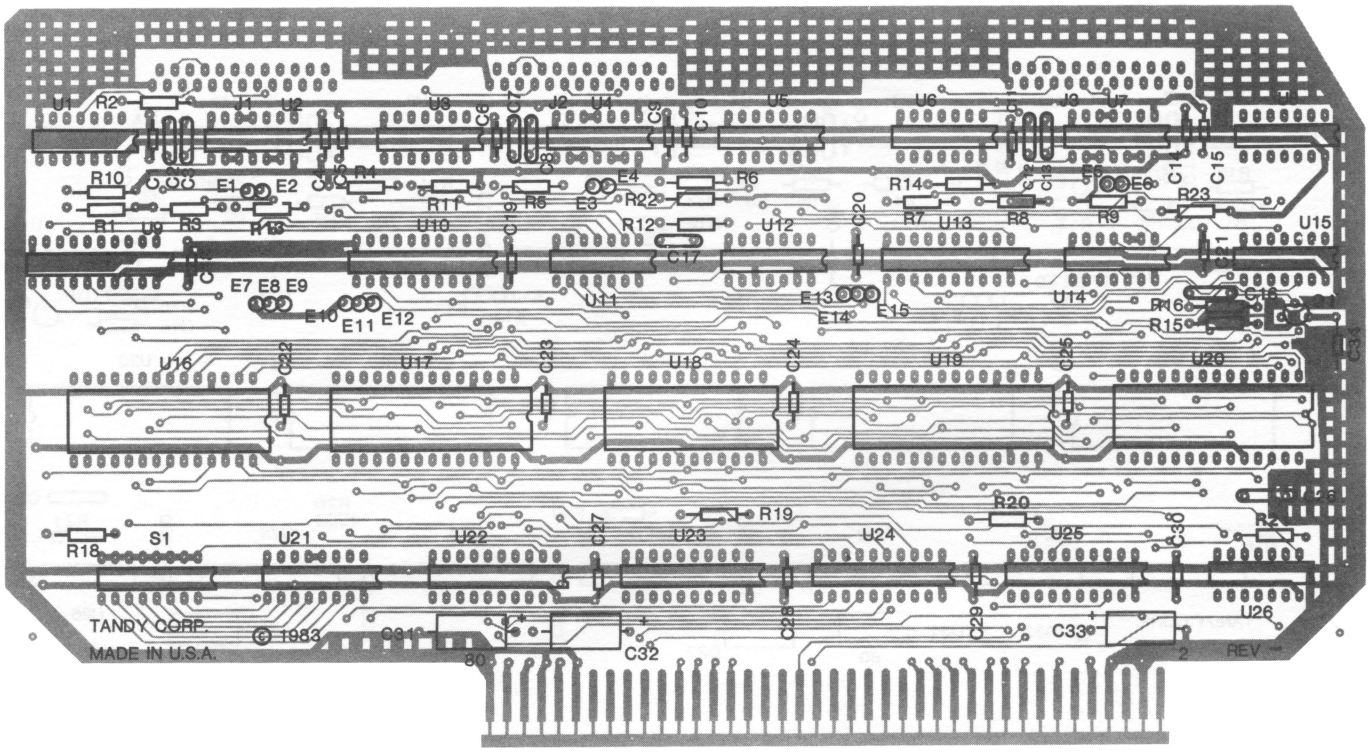


Schematic 8000198, Multiterminal Interface 26-6013

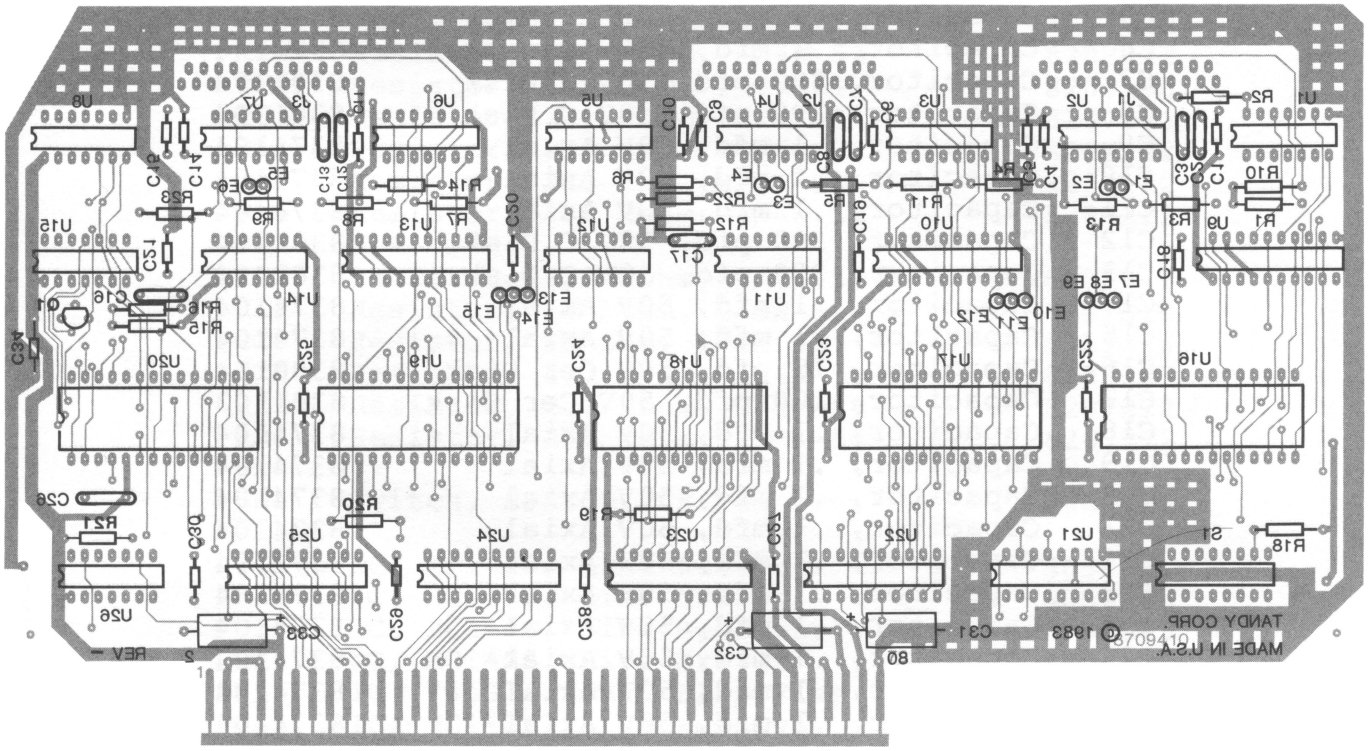
Schematic 8000188, Multiterminal Interface 26 8013



Component Layout, Multiterminal Interface Board 26-6013



Circuit Trace 1700230, Multiterminal Interface
Board 26-6013, Component Side



Circuit Trace 1700230, Multiterminal Interface
Board 26-6013, Solder Side

Parts List

Multiterminal Interface 26-6013

Item	Sym	Description	Part No.
	C1	Capacitor, .1 mfd,50V Axial	8374104
	C2	Capacitor, 390 pfd, 50V C Disk	8301394
	C3	Capacitor, 390 pfd, 50V C Disk	8301394
	C4	Capacitor, .1 mfd, 50V Axial	8374104
	C5	Capacitor, .1 mfd, 50V Axial	8374104
	C6	Capacitor, .1 mfd, 50V Axial	8374104
	C7	Capacitor, 390 pfd, 50V C Disk	8301394
	C8	Capacitor, 390 pfd, 50V C Disk	8301394
	C9	Capacitor, .1 mfd, 50V Axial	8374104
	C10	Capacitor, .1 mfd, 50V Axial	8374104
	C11	Capacitor, .1 mfd, 50V Axial	8374104
	C12	Capacitor, 390 pfd, 50V C Disk	8301394
	C13	Capacitor, 390 pfd, 50V C Disk	8301394
	C14	Capacitor, .1 mfd, 50V Axial	8374104
	C15	Capacitor, .1 mfd, 50V Axial	8374104
	C16	Capacitor, 15 pfd, 50V Cer Disk	8300154
	C17	Capacitor, 100 pfd, 50V Cer Disk	8301103
	C18	Capacitor, .1 mfd, 50V Axial	8374104
	C19	Capacitor, .1 mfd, 50V Axial	8374104
	C20	Capacitor, .1 mfd, 50V Axial	8374104
	C21	Capacitor, .1 mfd, 50V Axial	8374104
	C22	Capacitor, .1 mfd, 50V Axial	8374104
	C23	Capacitor, .1 mfd, 50V Axial	8374104
	C24	Capacitor, .1 mfd, 50V Axial	8374104
	C25	Capacitor, .1 mfd, 50V Axial	8374104
	C26	Capacitor, .1 mfd, 50V Axial	8374104
	C27	Capacitor, .1 mfd, 50V Axial	8374104
	C28	Capacitor, .1 mfd, 50V Axial	8374104
	C29	Capacitor, .1 mfd, 50V Axial	8374104
	C30	Capacitor, .1 mfd, 50V Axial	8374104
	C31	Capacitor, 10 mfd, 25V Elec Axial	8316102
	C32	Capacitor, 10 mfd, 25V Elec Axial	8316102
	C33	Capacitor, 22 mfd, 16V Elec Axial	8316221
	C34	Capacitor, .1 mfd, 50V Axial	8374104
	Q1	Transistor, 2N3906	8100906
	R1	Resistor, 2.2 kohm, 1/4W 5%	8207222
	R2	Resistor, 2.2 kohm, 1/4W 5%	8207222
	R3	Resistor, 2.2 kohm, 1/4W 5%	8207222
	R4	Resistor, 2.2 kohm, 1/4W 5%	8207222
	R5	Resistor, 2.2 kohm, 1/4W 5%	8207222

Parts List (cont)

Multiterminal Interface 26-6013

Item	Sym	Description	Part No.
	R6	Resistor, 2.2 kohm, 1/4W 5%	8207222
	R7	Resistor, 2.2 kohm, 1/4W 5%	8207222
	R8	Resistor, 2.2 kohm, 1/4W 5%	8207222
	R9	Resistor, 2.2 kohm, 1/4W 5%	8207222
	R10	Resistor, 2.2 kohm, 1/4W 5%	8207222
	R11	Resistor, 2.2 kohm, 1/4W 5%	8207222
	R12	Resistor, 560 ohm, 1/4W 5%	8207156
	R13	Resistor, 2.2 kohm, 1/4 5%	8207222
	R14	Resistor, 2.2 kohm, 1/4W 5%	8207222
	R15	Resistor, 220 ohm, 1/4W 5%	8207122
	R16	Resistor, 1.2 kohm, 1/4W 5%	8207212
	R17	N.A.	
	R18	Resistor, 4.7 kohm, 1/4W 5%	8207247
	R19	Resistor, 10 kohm, 1/4W 5%	8207310
	R20	Resistor, 56 ohm, 1/4W 5%	8207056
	R21	Resistor, 4.7 kohm, 1/4W 5%	8207247
	R22	Resistor, 2.2 kohm, 1/4W 5%	8207222
	R23	Resistor, 2.2 kohm, 1/4W 5%	8207222
	SW1	Switch, SPST DIP 8 Pos	8489004
	U1	IC, MC1489, Line Receiver	8050189
	U2	IC, MC1488, Line Driver	8050188
	U3	IC, MC1489, Line Receiver	8050189
	U4	IC, MC1488, Line Driver	8050188
	U5	IC, 74LS74, Dual Flip Flop	8020074
	U6	IC, MC1489, Line Receiver	8050189
	U7	IC, MC1488, Line Driver	8050188
	U8	IC, 74LS00, Quad 2-In NAND	8020000
	U9	IC, 74ALS241, Octal Buffer	8025241
	U10	IC, 74ALS241, Octal Buffer	8025241
	U11	IC, 74LS27, Triple 3-In NOR	8020027
	U12	IC, 74LS74, Dual Flip Flop	8020074
	U13	IC, 74ALS241, Octal Buffer	8025241
	U14	IC, 74LS04, Hex Inverter	8020004
	U15	IC, 74LS32, Quad 2-In AND	8020032
	U16	IC, 8251A, USART	8040251
	U17	IC, 8251A, USART	8040251
	U18	IC, 8253, Counter	8041253
	U19	IC, 8251A, USART	8040251
	U20	IC, Z8430A, CTC	8047882
	U21	IC, 74LS138, Decoder	8020138

Parts List (cont)

Multiterminal Interface 26-6013

Item	Sym	Description	Part No.
	U22	IC, 82S153	8040153
	U23	IC, 8303, Transceiver	8060303
	U24	IC, 74ALS240, Octal Buffer	8025240
	U25	IC, 74ALS244, Octal Buffer	8025244
	U26	IC, 7407, Hex Buffer	8000007
1	1	PCB Logic Board	8709410
2	15	Pin, Staking	8529014
3	2	Socket, 20 Pin DIP(U22,23)	8509009
4	1	Socket, 24 Pin DIP (U18)	8509001
5	4	Socket, 28 Pin DIP (U16,17 U19,20)	8509007
6	3	Connector, Rt Angle (J1-3)	8519109

4/ Troubleshooting

Correct installation of the Multiterminal Interface is ensured when the following commands typed into the computer running XENIX produce the noted responses.

Type in the following command*:

```
disable tty0X (enter)
```

Response

There will be no response of the following error message will appear:

```
disable: tty0X is already disabled
disable: /etc/ttys not updated     (which is OK)
```

Type in the following command:

```
cat /etc/ttys >/dev/tty0X (enter)
```

Response

```
lhconsole
09tty01
09tty02
09tty04
09tty05
09tty06
```

(or something similar -- it should look the same as if "cat /etc/ttys" were typed without any output redirection)

* 0X = one of the tty terminals, either 4, 5 or 6.
For example, tty04.

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